Birds PLD, Plan for Hardware Aspects of Certification

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Document BirdsPLD-PHAC, v1.00 07/09/2006

Signature	***Printed Name***	***Date***

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1. PHAC Modification History

Revision 0.00-0.99

Uncontrolled drafts.

2. Purpose of PHAC Document

This is a standard "Plan for Hardware Aspects of Certification" document, corresponding to the guidelines in RTCA DO-254. Among other things, it provides a system overview, a hardware overview, a description of the certification basis and justification, a description of the hardware development life cycle and data items, and a certification schedule.

3. Documentation Traceability to DO-254

BirdsPLD-PHAC	Plan for Hardware Aspects of Certification	DO-254 10.1.1
BirdsPLD-HDP	Hardware Design Plan	DO-254 10.1.2
BirdsPLD-HVVP	Hardware Validation and Verification Plan	DO-254 10.1.3 and 10.1.4
BirdsPLD-HCMP	Hardware Configuration Management Plan	DO-254 10.1.5
-	Hardware Process Assurance Plan, not needed at assurance level C	DO-254 10.1.6
-	Requirements Standards, not needed at assurance level C	DO-254 10.2.1
-	Hardware Design Standards, not needed at assurance level C	DO-254 10.2.2
-	Validation and Verification Standards, not needed at assurance level C	DO-254 10.2.3
-	Hardware Archive Standards, not needed at assurance level C	DO-254 10.2.4
BirdsPLD-HRD	Hardware Requirements Data	DO-254 10.3.1
BirdsPLD-HDRD	Hardware Design Representation Data	DO-254 10.3.2
BirdsPLD-HTPR	Hardware Test Processes and Results	DO-254 10.4.1, 10.4.4, and 10.4.5
-	Review Checklists	DO-254 10.4.2 and 10.4.3
BirdsPLD-VVD	Validation and Verification Data (collected filled-out HTPR and Review Checklists)	DO-254 10.4
BirdsPLD-HATC	Hardware Acceptance Test Criteria	DO-254 10.5
-	Problem Reports	DO-254 10.6
-	Hardware Configuration Management Records, combined with Validation and Verification Data (BirdsPLD-VVD)	DO-254 10.7
-	Hardware Process Assurance Records, combined with Validation and Verification Data (BirdsPLD-VVD)	DO-254 10.8
BirdsPLD-HAS	Hardware Accomplishment Summary	DO-254 10.9

4. PHAC Traceability to DO-254

This document organizes data in a manner consistent with DO-254 section 10.1.1, including the ordering of data and the section headings. In practice, the match is so obvious that there would be no benefit in having explicit section-by-section traceability to DO-254.

5. System Overview

5.1. System Functional Description

The system being developed is an crew-warning or annunciator system, in which activation of various electrical inputs causes annuciation of aural warnings. The system, referred to as the Birds Crew Warning System ("BirdsCWS") is CPU based.

However, this documentation deals only with the Programmable Logic Device (PLD) sub-system of the annunciator. The PLD sub-system, referred to as the "BirdsPLD", is present as a derived requirement. The BirdsCWS system requirements call for the use of a hardware architecture which is reusable across differing hardware generations or even to projects other than the BirdsCWS, in order to increase reusability of software libraries and documentation. Thus, as a derived requirement, the BirdsPLD is provided to help maintain constancy of hardware/software interfaces.

Considered as a system of itself, the BirdsPLD provides the following capabilities:

1. It interfaces to the CPU via the CPU's data/address bus.

2. It provides an 8-bit latched parallel-data output port.

3. It provides an 8-bit input parallel-data port.

4. It provides a watchdog timer which can be disabled via a signal intended to be controlled by a hardware jumper.

5. It provides decoding for some peripheral devices.

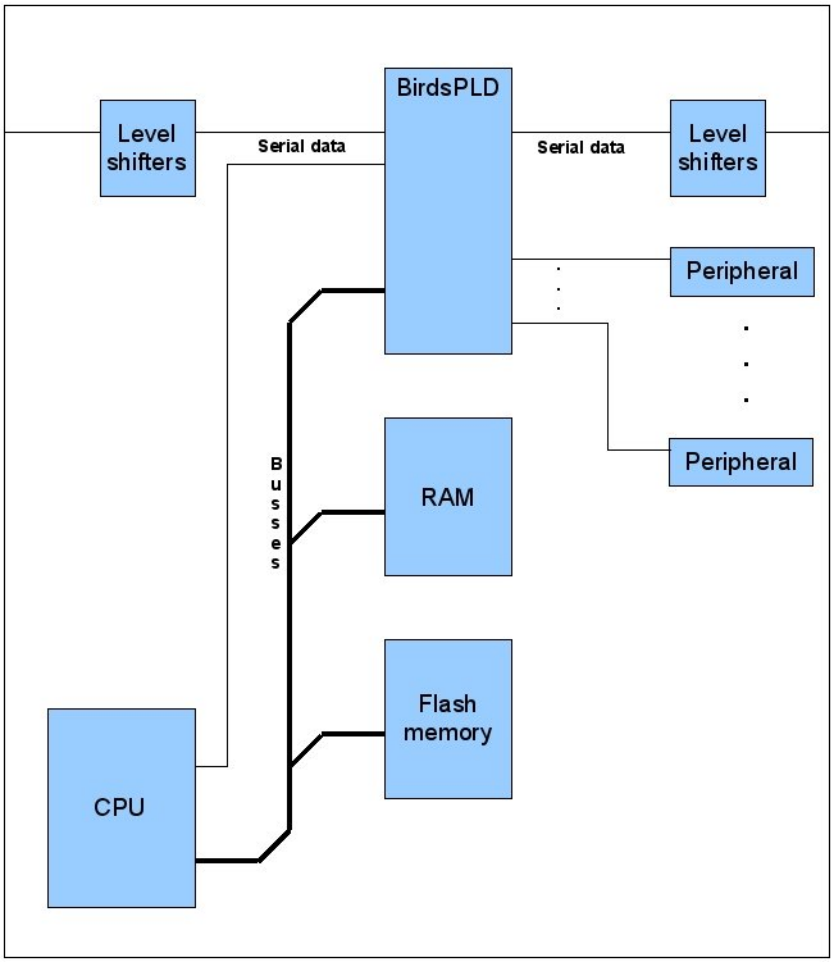
6. It provides for flexible routing of serial data on the basis of electrical signals intended to be controlled via DIP switches.

Although the BirdsCWS CPU may itself have some of these facilities embedded within it, using the BirdsPLD rather than the embedded capabilities of the CPU allows much more flexibility in choice of CPU without software change. This is because it is much easier to replace the CPU with one having a 100% compatible instruction set rather than one with 100% compatible peripheral devices.

5.2. System Failure Conditions

There are no identifiable failure conditions of the BirdsPLD sub-system.

5.3. System Architecture



BirdsCWS Block Diagram

5.4. Allocation of Functions to Hardware and Software

The BirdsPLD is a derived requirement, implemented entirely in hardware.

5.5. Allocation of Safety Requirements to Hardware and Software

There are no safety requirements associated with the BirdsPLD.

5.6. Other System Documentation

The BirdsCWS (for which the BirdsPLD is a derived requirement) system requirements are described in Birds Project document BirdsCWS-SCD.

6. Hardware Overview

6.1. Hardware Functional and Performance Requirements

6.1.1. Interface to CPU

6.1.1.1. Synopsis

Registers internal to the BirdsPLD interface to the CPU via the CPU's address/data/control bus. Each of these internal registers is 8 bits in width. A single chip-select signal from the CPU is used, and the BirdsPLD internally decodes 4 address signals and a read/write control line to select the specific registers and the data direction.

6.1.2. Parallel Output Port

6.1.2.1. Synopsis

The BirdsPLD has a single internal 8-bit register (see "Interface to CPU" above) which, upon being written to by the CPU, latches the data and delivers it to 8 discrete output pins of the BirdsPLD. The register may also be read by the CPU, in which case the contents of the latch are returned.

6.1.3. Parallel Input Port

6.1.3.1. Synopsis

The BirdsPLD has an 8-bit register (see "Interface to CPU" above) which can be interrogated by the CPU to determine the state of 8 discrete input signals to the BirdsPLD.

6.1.4. Watchdog Timer

6.1.4.1. Synopsis

The BirdsPLD implements a watchdog timer circuit which must be refreshed periodically or else it times out and generates an output signal intended to be used as a system reset. Refreshing the watchdog involves the CPU writing two predetermined valued to two internal 8-bit registers (see "Interface to CPU" above) of the BirdsPLD.

6.1.5. Peripheral Address Decoder

6.1.5.1. Synopsis

The BirdsPLD provides address decoding for 8 peripheral devices external to the CPU and BirdsPLD. It employs the same chip-select as for "Interface to CPU" above, conditions that chip-select by detecting that the address lines are in 8 different address ranges, and outputs 8 sets of control signals.

6.1.6. Serial Data Routing

6.1.6.1. Synopsis

The BirdsPLD accepts 4 serial-data signals as inputs and outputs 4 serial-data signals as outputs. For each of the 4 outputs, there are 2 input signals determining which of the 4 inputs is routed to the output.

6.2. Hardware Reliability and Quality Requirements

None.

6.3. Hardware Maintenance and Repair Requirements

None.

6.4. Hardware Manufacturability and Assembly Requirements

None.

6.5. Hardware Testability Requirements

None.

6.6. Hardware Storage and Handling Requirements

None.

6.7. Installation Requirements

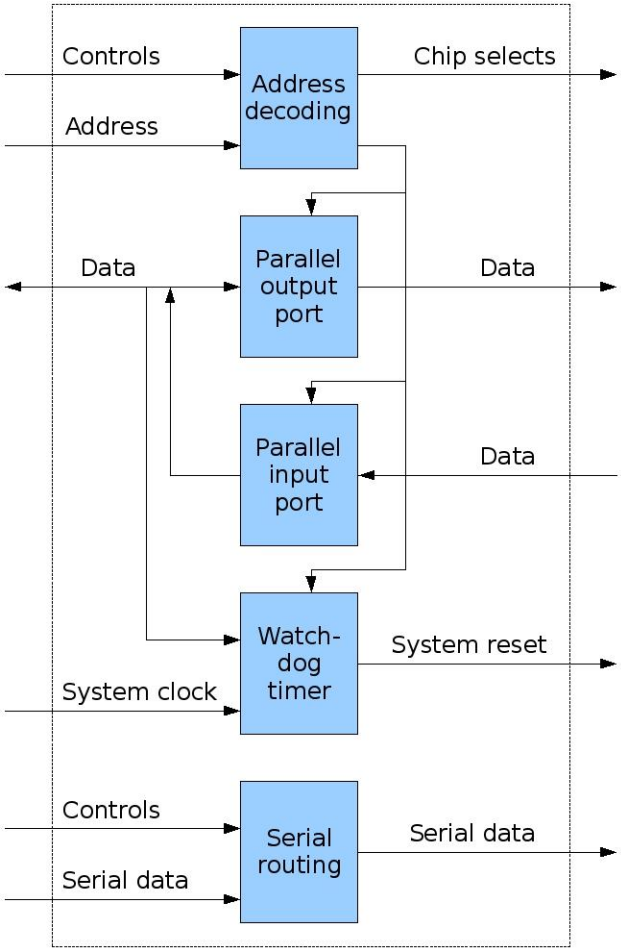
None.

6.8. Hardware Items

6.8.1. BirdsPLD

The sole hardware item covered by this documentation is the BirdsPLD itself.

6.9. Hardware Architecture



BirdsPLD Block Diagram

6.10. New Technologies

None.

6.11. Fail-Safe Techniques

None.

6.12. Fault Tolerance Techniques

None.

6.13. Redundancy Techniques

None.

6.14. Partitioning Techniques

Each function of the BirdsPLD is implemented at a DO-254 assurance level of C. Thus there is no partitioning of assurance levels.

7. Certification Considerations

7.1. Summary of the Certification Basis

Please reference the documentation of the parent BirdsCWS project (BirdsCWS-PHAC).

7.2. Means of Compliance

RTCA DO-254 is used as the means of compliance, per FAA AC20-152.

7.3. Hardware Level

The assurance level is C. (Refer to RTCA DO-254, Table 2-1.)

7.4. Justification of Hardware Level

Please reference the documentation of the parent BirdsCWS project (BirdsCWS-PHAC).

8. Life Cycles

8.1. BirdsPLD Hardware Development Life Cycle

8.1.1. Life-Cycle

8.1.1.1. Processes

The Hardware Design Plan (HDP) describes the life-cycle processes in detail. What follows is a brief summary.

The canonical life-cycle processes envisaged by DO-254 Chapter 3 are used. The following processes occur in sequential order:

- Planning Process
- Requirements Capture Process, wherein system requirements are allocated to hardware requirements, and traceability between system requirements and hardware requirements is established.
- Conceptual Design Process, wherein hardware requirements are developed in detail.
- Detailed Design Process, wherein specific design artifacts such as schematic captures, bills of material, or HDL source code are developed from the conceptual design data.
- Implementation Process, wherein detailed design data is converted to physical hardware such as circuit boards or ASICs.
- Validation and Verification Process. The "validation" portion of this process actually is concurrent with all other process, and only the "verification" part is sequential. However, validation occurs by means of review checklists called out by process checklists of the other processes. In other words, validation is really integrated with other processes rather than being a separate process of itself.

- Product Transition Process, wherein manufacturing and repair data is created, traceability with detailed design data is established, and acceptance occurs.

The following processes are concurrent with the sequential processes:

- Hardware Configuration Management Process
- Hardware Process Assurance
- Certification Liaison Process

8.1.1.2. Process Procedures

The Hardware Design Plan (HDP) describes the process procedures in detail. What follows is a brief summary.

Each of the hardware life-cycle process (Planning, Requirements Capture, etc.) has an associated checklist which itemizes each of the steps required to complete that process. The checklists are separate documents, called out in the Hardware Development Plan (HDP). The checklists include not only the steps specific to the associated processes, but also all of the Validation Process, Hardware Configuration Management Process, and Certification Liaison steps which are relevant, thus obviating most of the need for separate Validation, Hardware Configuration Management, and Certification Liaison Processes. Additionally, the checklists contain some, but not all, associated Hardware Process Assurance tasks.

At the outset of any given life-cycle process, the lead hardware developer obtains a blank copy of the process checklist. As each step of the process is performed, the he/she initials and dates that step. When all steps are complete, or when a regression is made to an earlier life-cycle process, the completed process becomes part of the Hardware Process Assurance Records (HPAR), which for this project are combined with the Validation and Verification Data (VVD). When a regression to an earlier life-cycle process is made, the lead developer obtains a new, blank copy of the earlier life-cycle process.

Blank life-cycle process checklists are reviewed and approved, prior to use, by the lead hardware developer. In case the life-cycle processes are identical to those in previously-developed hardware at the same assurance level, process checklists from the prior project can be used unchanged.

Hardware Process Assurance (HPA) differs from the other life-cycle processes, in that it does not have a process checklist. Rather the process checklists lists all relevant HPA tasks. Since DO-254 does not require formal HPA at assurance level C, all HPA activities are performed by the lead hardware developer.

8.1.1.3. Hardware Design Methods

Hardware requirements, design, test procedures, and configuration data are captured and interrelated using a software tool called **Do178Builder**.

Conceptual design data is converted to detailed design data by creating VHDL source code, and then compiling that code using tools provided by the manufacturer of the PLD device used.

8.1.1.4. Process Standards

None.

8.1.1.5. Activities

The activities are defined by the Hardware Design Plan (BirdsPLD-HDP). In brief, each development process (Planning, Requirements Capture, Conceptual Design, etc.) has an associated checklist of activities, managed by the lead

hardware developer. The checklist for each development process is completed before proceeding to the next development process. The process checklists include: development of data items, review and release of data items, etc.

8.1.1.6. Organizational Responsibilities

The BirdsPLD is solely developed by Ron Burkey of the Birds Project.

8.1.2. Life-Cycle Data

8.1.2.1. Data Items

BirdsPLD-PHAC	Plan for Hardware Aspects of Certification	Planning	Submit
BirdsPLD-HDP	Hardware Design Plan	Planning	Records
BirdsPLD-HVVP	Hardware Validation and Verification Plan	Planning	Submit
Birds-HCMP	Hardware Configuration Management Plan	Planning	Records
-	Note that a Hardware Process Assurance Plan is not needed at assurance level C.	-	Not used
-	Note that Requirements Standards are not needed at assurance level C.	-	Not used
-	Note that Hardware Design Standards are not needed at assurance level C.	-	Not used
-	Note that Validation and Verification Standards are not needed at assurance level C.	-	Not used.
-	Note that Hardware Archive Standards are not needed at assurance level C.	-	Not used.
BirdsPLD-HRD	Hardware Requirements Data	Requirements Capture	Records
BirdsPLD-HDRD	Hardware Design Representation Data	Conceptual Design	Records
-	Detailed Design Data	Detailed Design	Submit top-level drawing only
BirdsPLD-HT-PR	Hardware Test Processes and Results	Verification	Records
BirdsPLD-VVD	Validation and Verification Data	Validation and Verification	Records
BirdsPLD-HATC	Hardware Acceptance Test Criteria	Verification	Records
BirdsPLD-HAS	Hardware Accomplishment Summary	Product Transition	Submit
-	Hardware Configuration Management Records are combined with the Validation and Verification Data (BirdsPLD-VVD)	Configuration Management	Records
-	Hardware Process Assurance Records are combined with the Validation and Verification Data (BirdsPLD-VVD)	Process Assurance	Records

9. Additional Considerations

9.1. Previously-Developed Hardware

None. Note that the BirdsPLD is being developed in a manner that presumes it will eventually be possible to use it as previously-developed hardware in other projects.

9.2. Commercial Off-the-Shelf Hardware

None.

9.3. Product Service-History

None.

9.4. Tool Assessment and Qualification

Outputs of all tools are checked as part of the Verification Process, and therefore the tools themselves do not need qualification.

Note, however, that the traceability data is automatically generated by the documentation tool (**Do178Builder**) used to manage the requirements, the design data, and the test procedures, and that it would be very convenient to be able to use this data as-is without the burden of having to check it. Since the **Do178Builder** tool is not qualified for this purpose initially, manual checks of the traceability data will have to be made for the initial release of the BirdsPLD. However, this initial check shall qualify the **Do178Builder** tool (in the version used for the initial release) for generation of traceability data in later releases of the BirdsPLD or other Birds Projects hardware development.

9.5. Alternative Methods of Compliance

No methods of compliance other than those of DO-254 are used.

10. Certification Schedule

Reference the documentation of the parent project (BirdsCWS-PHAC). Activities related solely to the BirdsPLD sub-project are as follows.

Date	Milestone	Comment
August 2006	DER accepts PHAC	
September 2006	HDP, HVVP, HCMP ready	
October 2006	HRD, HDRD ready	
November 2006	Detailed design and implementation complete	
December 2006	Test procedures (HTPR) complete	
January 2007	Testing complete	
February 2007	DER signoff, BirdsPLD released	

11. Glossary

ASIC. Application Specific Integrated Circuit.

CAD. Computer Aided Design.

CAM. Computer Aided Manufacturing.

COTS. Commercial Off-The-Shelf.

CPLD. Complex Programmable Logic Device.

DER. Designated Engineering Representative.

FAA. Federal Aviation Administration.

FPGA. Field Programmable Gate Array.

HARS. Hardware Archiving Standards.

HATC. Hardware Acceptance Test Criteria.

HAS. Hardware Accomplishment Summary.

HC1 and **HC2**. Hardware Control Categories 1 and 2.

HCM. Hardware Configuration Management.

HCMP. Hardware Configuration Management Plan.

HCMR. Hardware Configuration Management Records.

HDL. Hardware Description Language or Hardware Design Language. For example, Verilog, VHDL, Abel.

HDP. Hardware Design Plan.

HDRD. Hardware Design Representation Data.

HDS. Hardware Design Standards.

HPA. Hardware Process Assurance.

HPAP. Hardware Process Assurance Plan.

HPAR. Hardware Process Assurance Records.

HRD. Hardware Requirements Data.

HTPR. Hardware Test Procedures and Results.

HVVP. Hardware Validation and Verification Plan.

ICD. Interface Control Drawing.

LRU. Line Replaceable Unit.

PCB. Printed Circuit Board. Same as PWB. I.e., a "bare" circuit board as fabricated, prior to assembly with electronic components.

PHAC. Plan for Hardware Aspects of Certification.

PLD. Programmable Logic Device.

PR. Problem Report(s).

PWA. Printed Wire Assembly. I.e., a PCB or PWB after assembly with electronic components.

PWB. Printed Wire Board. Same as PCB. I.e., a "bare" circuit board as fabricated, prior to assembly with electronic components.

RTCA. Once upon a time, Radio Technical Commission for Aeronautics. Now, apparently, simply "RTCA, Inc." without being intended as an acronym.

SCD. Specification Control Drawing.

RS. Requirements Standards.

VVS. Validation and Verification Standards.